ABSTRACT

The subject invention is an electronic phase-locked loop for the jitter-attenuated generation of an output clock signal which is phase-synchronous with respect to a reference clock signal. The phased lock loop is a digitally controllable oscillator with a drive circuit connected to a digitally controllable oscillator for digitally setting the output clock signal of the digitally controllable oscillator so that a phase error between the output clock signal and a reference clock signal is zero. A digital phase detector compares the output clock signal of the oscillator with the reference clock signal, an analog phase detector, and a lock detection circuit connected to a digital phase detector and an analog phase detector for avoiding a phase quantization error. The lock detection circuit activates the analog phase detector to run simultaneously with a digital phase detector if the phase error is zero. The activated analog phase detector regulates the output clock signal of the digitally controllable oscillator in a continuously variable manner until the respective clock signal edges of the output clock signal and the reference clock signal are fully synchronous. The lock detection circuit deactivates the analog phase detector and continuously checks and regulates the digital phase detector until the phase error between the output clock signal and the reference clock signal is zero.